

EXHIBIT A

p910328

TITLE OF INVENTION

Definition of the contact area of electrode and phase change material in the chalcogenide phase-change memory

BEST AVAILABLE COPY

CLASSIFICATION: Method

SUITABLE PRODUCT: Chalcogenide
Memory (Next generation memory)

(This page will be provided by IPO)

BACKGROUND OF THE INVENTION

Field of the invention

- The invention describes a novel method to fabricate ultra-small contact area between electrode and phase change material in the chalcogenide phase change memory. With this method, the contact area of the chalcogenide part and electrode will be ultra small, and as a result the current/power requirement of the chalcogenide memory dramatically decreases. The contact area of the chalcogenide part and electrode is defined by the thin film process and etching process in this invention.

The issues were solved and improved by the invention

- It is known that the chalcogenide phase change memory is not easy to be driven by CMOS circuit, because chalcogenide requires relatively high current to change its phase. Reducing the cross-sectional area of chalcogenide or electrode can reduce the current requirement directly. Many structures have been invented to reduce area. For example, to fabricate a ultra-small contact hole and place the chalcogenide into the contact. However, these inventions basically are limited by lithography. Furthermore, it is very difficult to place materials into ultra-small and deep holes. In this invention, contact area of the chalcogenide part and electrode is defined by the thin film process and etching process. Therefore, the lithography is no longer the limit. It is also not necessary to place materials into ultra-small holes. Moreover, contact area of the chalcogenide part and electrode is ultra-small. As a result, the current/power requirement of the chalcogenide memory is dramatically decreased.

SUMMARY OF THE INVENTION

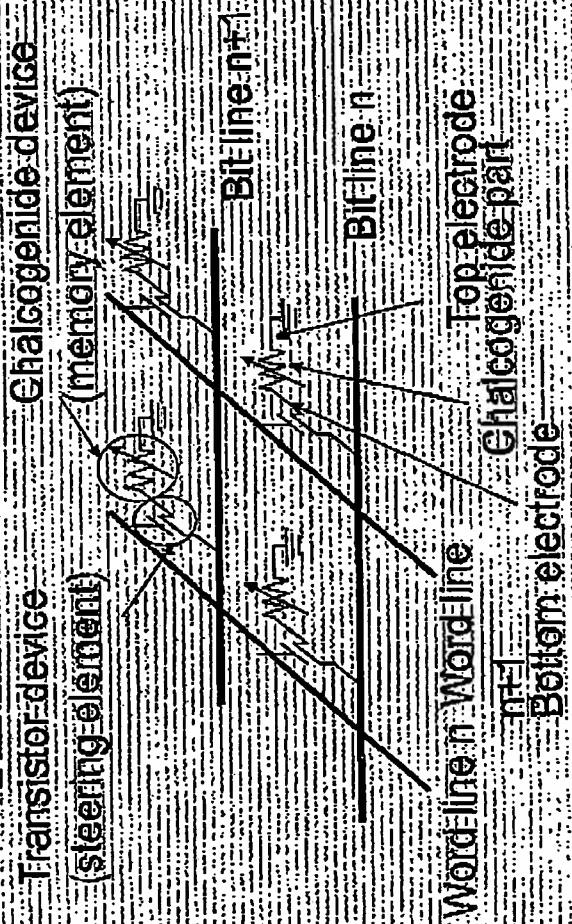
□ How this invention solves existing problems and achieves the objects

■ The contact area of the chalcogenide part and electrode is defined by 1. electrode film thickness and 2. The thickness of pad layer. With well control of film thickness, the area will be very small. Therefore the current required in the chalcogenide phase-change memory is reduced.

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

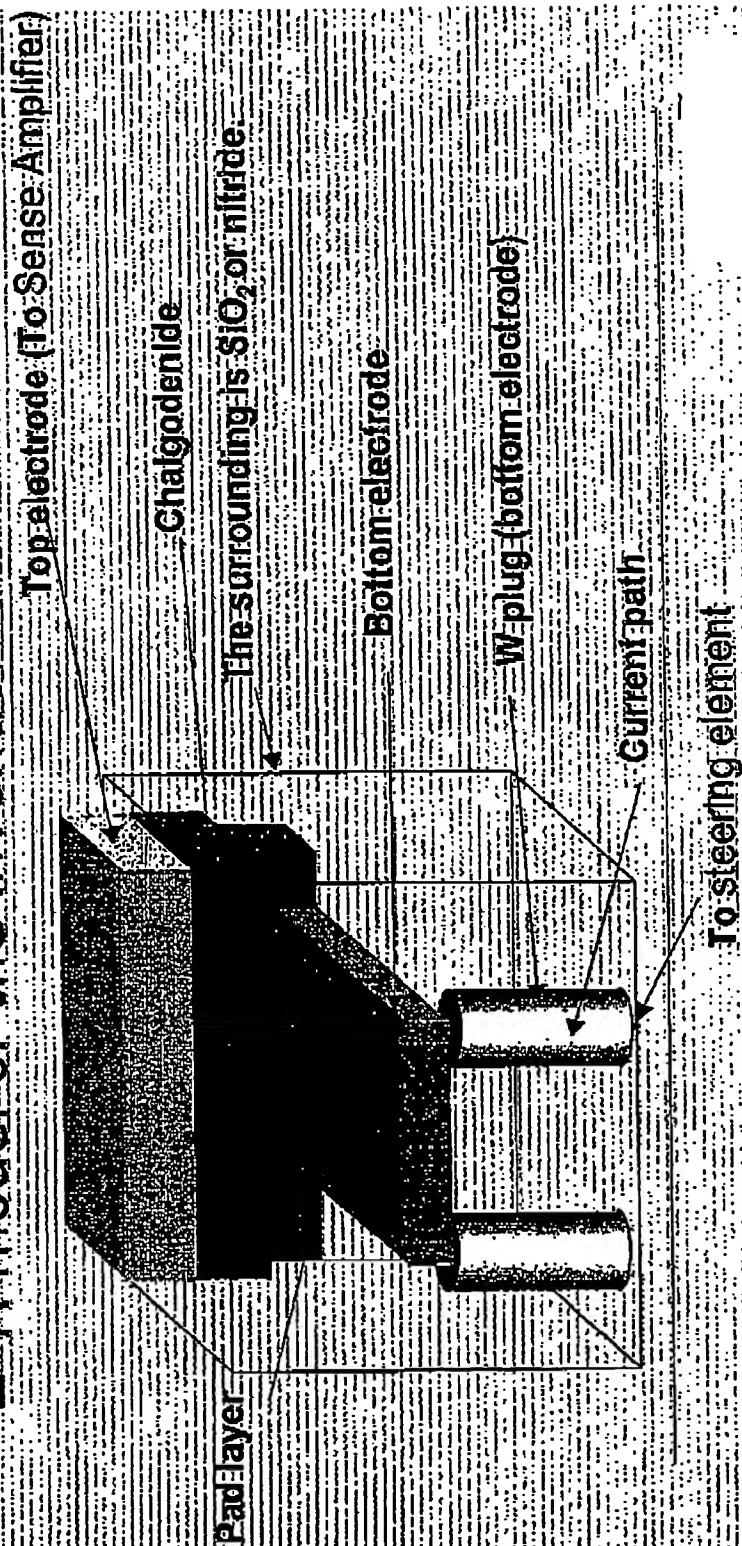
- A drawing of typical chalcogenide memory array.



BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

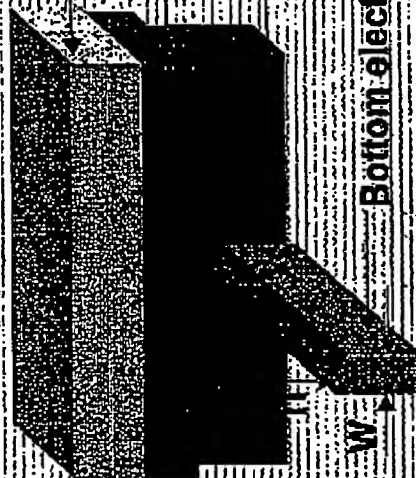
- A model of the invention.



BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

■ A model of the invention.



Top electrode (To Sense Amplifier)

Chalcogenide

Contact region between
chalcogenide and electrode

Bottom electrode

The width and height of the contact region between
chalcogenide and electrode are defined by thin film
and etching processes.

W: width of the bottom electrode.

H: height of the bottom electrode.

L: length of the bottom electrode.

BRIEF DESCRIPTION OF DRAWING

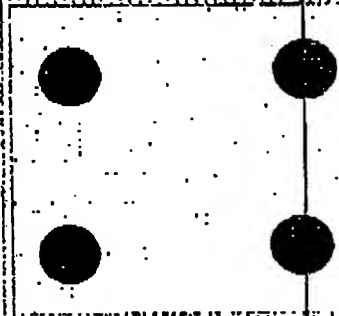
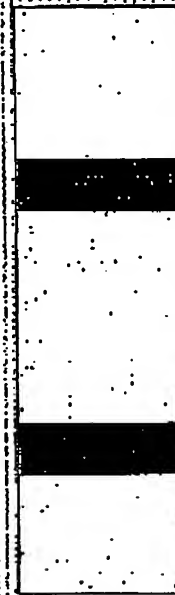
RELATED DRAWINGS

■ Process flow

□ After regular CMOS process and W plug

AA' cross-section

Plan view (4 cells)

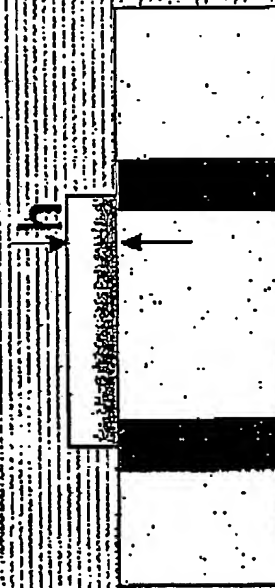


BRIEF DESCRIPTION OF DRAWING

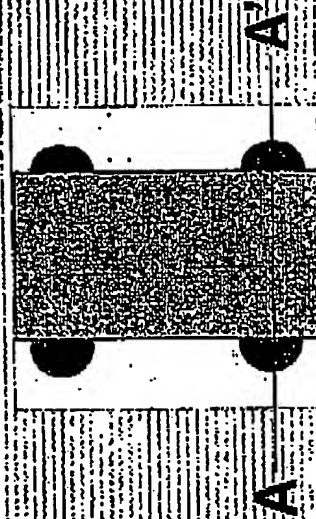
RELATED DRAWINGS

- Pad layer (SLAB/ PHOTO/ ETCHING) Pad layer can be SiN, SiO₂, or SiON, etc...
- This process defines the height (h) of the bottom electrode.

AA' cross-section



Plan view (4 cells)



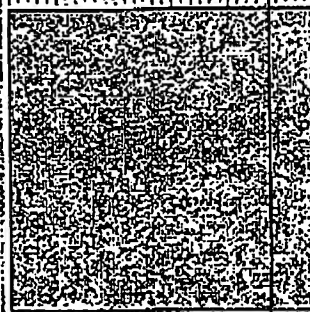
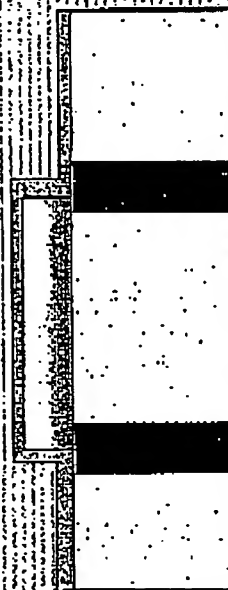
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- bottom electrode layer deposition (it can be TaN, TiN, TiW, Ti, W, poly or the combinations of above)

AA' cross-section

Plan view (4 cells)



A'

A

BRIEF DESCRIPTION OF DRAWING

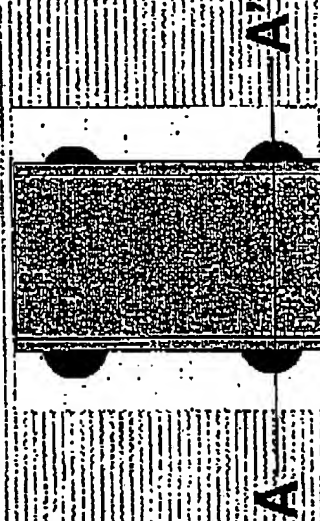
RELATED DRAWINGS

- Etching Back of bottom electrode
- Current and last processes define the width (w) of the chalcogenide part.

AA' cross-section



Plan view (4 cells)



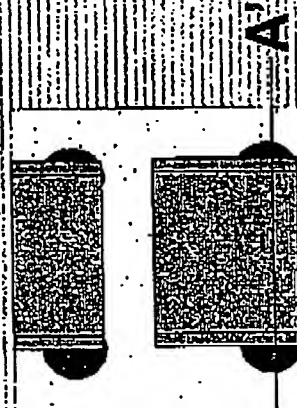
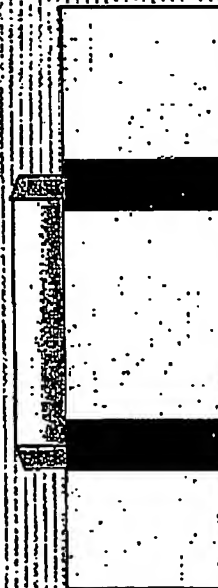
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

□ Bottom electrode cutting (Photo/Etching)

AA' cross-section

Plan view (4 cells)



BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

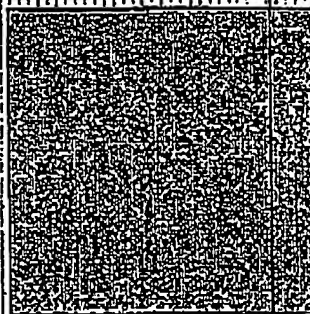
Cap-layer Deposition (it can be SiON, SiO₂, ZnS-SiO₂, etc.)

AA' cross-section

Plan view (4 cells)



A



A'

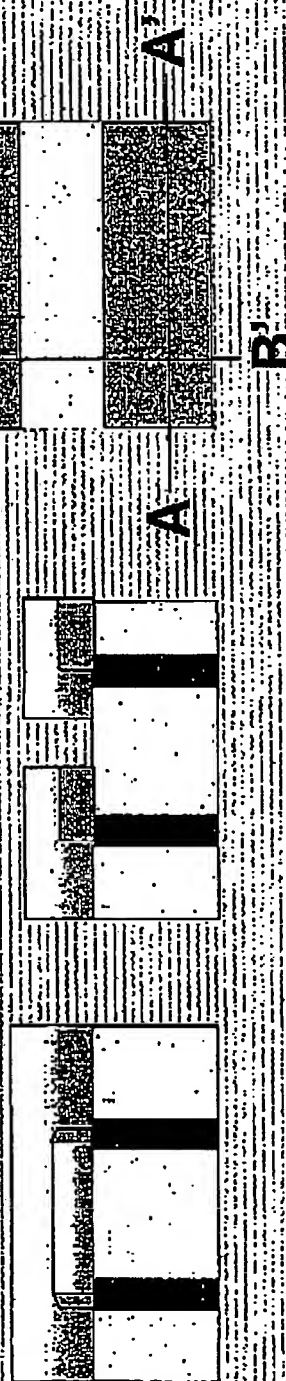
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Routing: Photo/Etching
- Etching process should cut the electrode again.
- This process defines length (L) of the bottom electrode

Plan view (4 cells)

AA' cross-section BB' cross-section



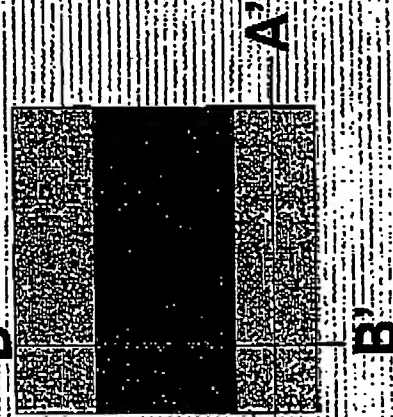
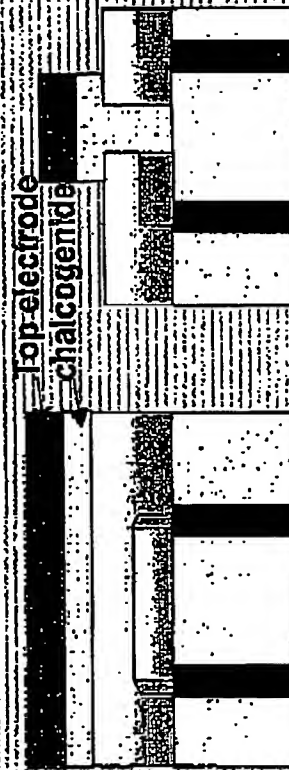
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Routing 2: Chalcogenide and top electrode dep/
Photo/Etching

Plan view (4 cells)

AA' cross-section BB' cross-section



PRIOR ART REFERENCE

classification	Patent No	Title	Remark
Prior art 1	US6111264	Small pores defined by a disposable internal spacer for use in chalcogenide memories	Similar to US6189582
Prior art 2	US6031287	Contact structure and memory element incorporating the same	
Prior art 3	US6114713	Integrated circuit memory cell having a small active area and method of forming same	

• CATEGORY: ESSAY, PAPER, PATENT, PRODUCT, ETC

COMPARING RELATED PRIOR ART WITH THIS INVENTION

Prior art 1	Disadvantages of the Related Prior art	Differences from this invention
Prior art 1	<p>1- Dielectric layer can reduce the pore size, but the etching ratio is not unlimited. Because overhang may seal the hole. Therefore, the pore size can be limited by lithography. It is difficult to scale down.</p> <p>2- It is very difficult to control the size uniformity of ultra small pores with this method.</p> <p>3- It is very difficult to place chalcogenide into the holes.</p>	<p>1- The current is limited by chalcogenide.</p> <p>2- The minimal current path cross sectional area is defined by photo thin film etching processes.</p>

COMPARING RELATED PRIOR ART WITH THIS INVENTION

	Disadvantages of the related Prior art	Difference from this Invention
Prior art 2	<p>1. Electrode area can be reduced by this method, but the shrinkage ratio is limited by the film thickness and photo. For example, if pore diameter is 0.15 μm and film thickness is 200A, the shrinkage ratio is only about 80%. It is difficult to scale down.</p> <p>2. Because the process needs to place electrode and oxide into small contacts, it is very difficult to process.</p>	<p>1. The bottom electrode is vertical and placed in a hole.</p> <p>2. The cross-sectional area of chalcogenide is defined by photothin film processes.</p>

COMPARING RELATED PRIOR ART WITH THIS INVENTION

Prior art 3	Disadvantages of the related Prior art	Difference from this invention
	1. It is very difficult to control the electrode area	1. The cross-sectional area of the electrode is defined by photo etching processes

THE SCOPE OF THE PROTECTION OF THE PATENT

■ Main Feature of the Invention

- The contact area between the chalcogenide and electrode is defined by 1. electrode film thickness and 2. The thickness of pad layer. With well control of film thickness, the area will be very small. Therefore the current required in the chalcogenide phase change memory is reduced.

■ The advantages of the invention

- Ultra small contact area between the chalcogenide and electrode.
- Easy to fabricate. (Do not need to place materials into small pores)
- Easy to scale down. (The scaling limit of thin film and etching is less than 50A in 0.25um technology.)
- Take an easy calculation as an example:
If the PAD layer thickness is 500A and the electrode layer thickness is 200A, which is easy to fabricate by 0.25um process, the contact area is less than 10⁻⁵ A². This is the cross section of a 0.036 um contact, which is almost impossible to fabricate nowadays.



**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

☐ **BLACK BORDERS**

☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**

☐ **FADED TEXT OR DRAWING**

☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**

☐ **SKewed/SLANTED IMAGES**

☒ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**

☐ **GRAY SCALE DOCUMENTS**

☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**

☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**

☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.